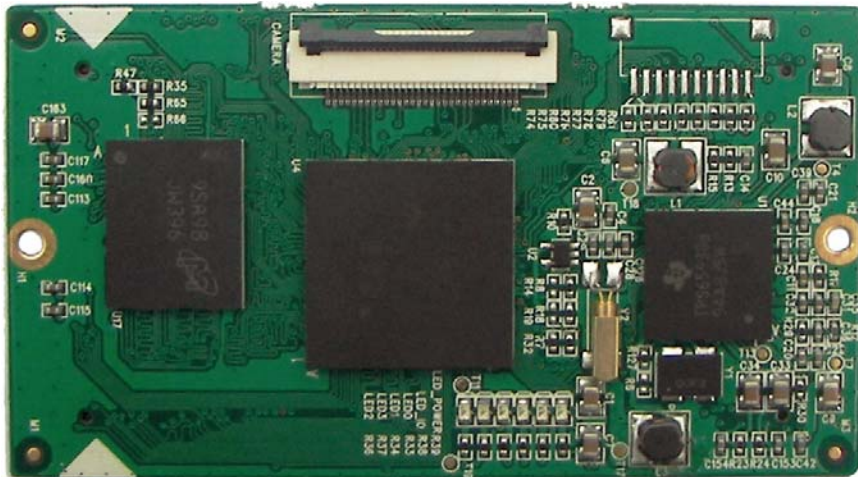


Mini8100 核心板

Mini8100是天漠科技推出的一款基于OMAP3530 的嵌入式核心模块，预装Linux2.6 多任务操作系统，用户可根据核心板硬件接口定制开发出自己的外设产品底板，也可在配套底板【SBC8100】的设计基础上快速地进行功能的裁剪，实现用户的产品快速上市。

Mini8100 支持Linux 2.6.29 及Wince6.0 操作系统，并提供linux2.6.29 源码及wince6.0 BSP 源码包，用户可根据自己定制的底板硬件特点，对linux及wince系统进行功能裁剪，更快的开发出适合自己的产品。



硬件特性

CPU 单元:

- OMAP3530 应用处理器，核心频率 600MHz（Pin to Pin 兼容 OMAP3503，OMAP3515，OMAP3525 处理器）
- 600-MHz ARM Cortex-A8 Core
- 430-MHz TMS320C64x+ DSP Core
- 256MByte DDR SDRAM
- 256MByte NAND Flash
- 6 层板

通讯接口:

- 提供 2 路 SPI:SPI1、SPI2
- 提供 GPMC 总线（16 位数据、10 位地址、4 个片选、控制信号若干）
- 提供三路 UART:（5 线，支持硬件流控）
- 提供一路 ULPI:（USB1 HS）
- 提供音频输入/输出接口
- 支持 12 位 CAMERA 接口（可外接 CCD 和 CMOS 的摄像头）
- 提供 1 路 IIC
- 提供 2 路的 McBSP: McBSP1、McBSP3（McBSP3 与 UART2 复用）
- 支持 2 路 MMC/SD: MMC1（8 线）、MMC2（4 线）

- 提供 24 位 DSS 接口

显示单元:

- 1 个 DVI 接口 (芯片: TFP410), 可输出分辨率 1280x720, 码率 30fps 的 DVI-D 高清信号
- 24bit 真彩色 LCD 接口 (含 4 线触摸屏接口, 分辨率可支持 2048x2048)

电气参数:

- 工作温度: 0 ~ 70°C (芯片支持)
- 环境湿度: 20% ~ 90% , 非冷凝
- 机械尺寸: 67 mm * 37 mm
- 电气指标: +3.3V 电源供电, 电流 170mA
- 功耗: 0.17@ 3.3V

软件特性

Linux 系统特性:

- Linux 版本: Linux2.6.29
- 编译器版本: gcc version 4.2.1 (CodeSourcery Sourcery G++ Lite 2007q3-51)
- 启动方式: 支持网络、SD 卡或 NAND Flash 中启动引导 Linux 系统
- 更新方式: 支持网络或 SD 卡更新映像
- 文件系统格式: Ramdisk 文件系统、UBI 文件系统
- 文件系统支持: ROM/CRAM/EXT2/EXT3/FAT/NFS/JFFS2/UBIFS
- 设备管理支持: udev 设备管理
- 驱动支持: Serial, RTC, NAND, DVI, LCD, 触摸屏, SD 卡, USB OTG(作从设备), 键盘, 音频, 网络, LED, GPS, WIFI

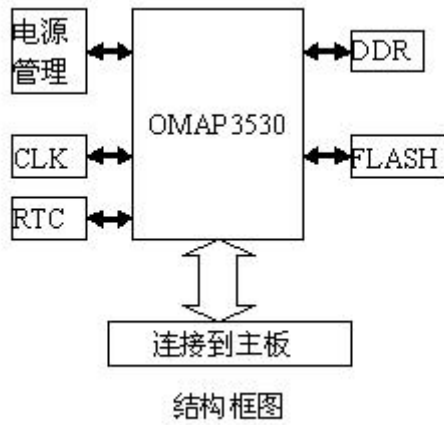
Wince 系统特性:

- Wince 版本: Wince6.0
- 启动方式: 网络、SD 卡或 NAND Flash 中启动引导 wince 系统
- 更新方式: 网络或 SD 卡更新映像
- 文件系统: 支持 HIVE 注册表支持及 ROM 文件系统 (可读写)
- 系统特性: 支持.NET Compact Framework 3.5 及 KITL 内核调试
- 电源管理: 背光管理、电池管理、休眠\唤醒功能
- 支持微软的远程调试工具对目标板的文件、注册表、进程及线程的管理
- 驱动支持: DVI, LCD, SD 卡, 键盘, 音频, 网络, NLED, USB OTG, USB HOST (作主设备), RTC, Watchdog, GPS, WIFI

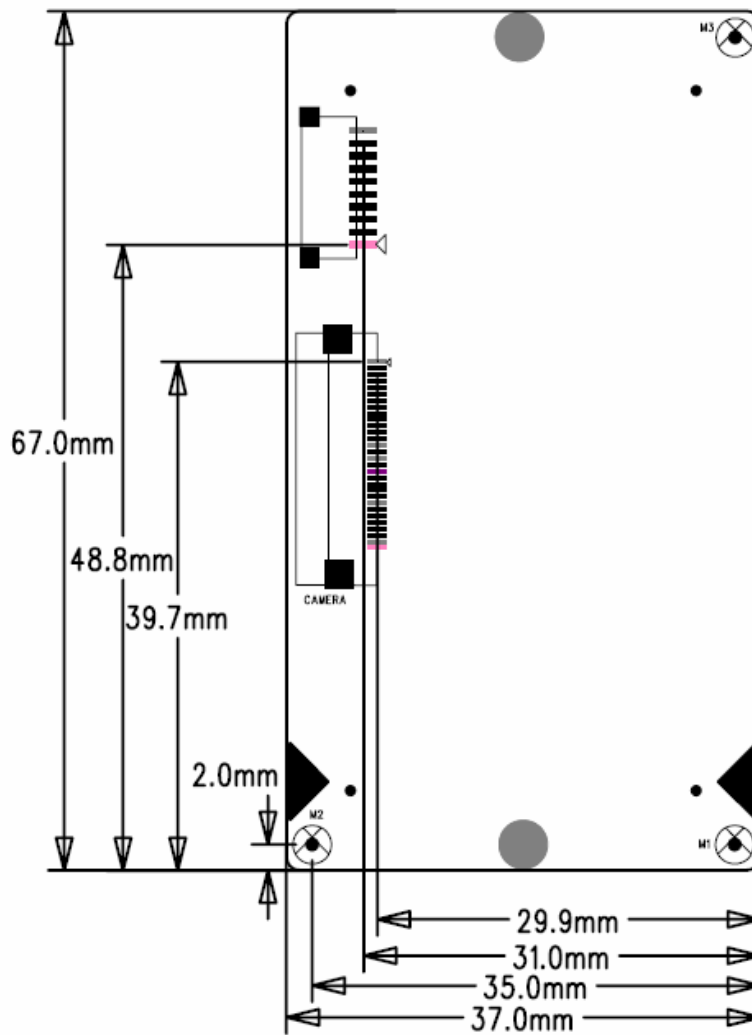
提供文件:

- 提供已编译好的 WinCE 镜像文件
- 提供已编译好的 Linux 镜像文件
- 提供接口定义

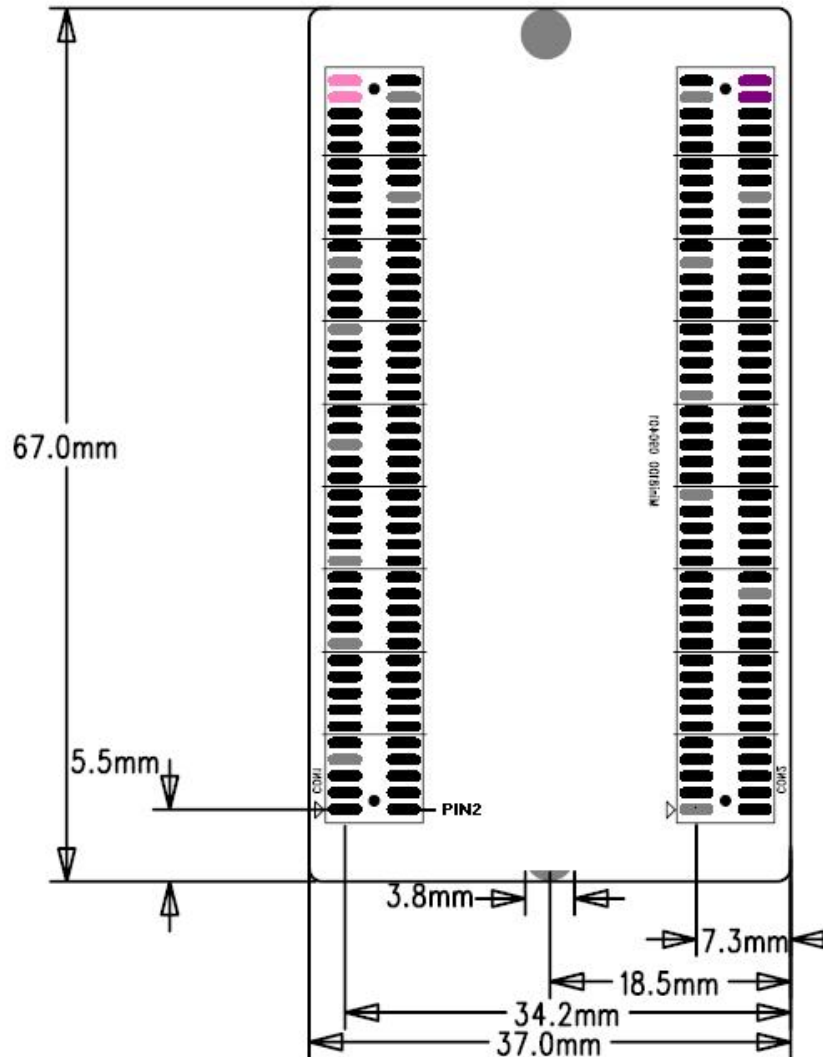
结构框图



尺寸规格



Mini8100 top layer



Mini8100 Bottom layer

摄像头接口

该接口是一个 30pin 的 FPC 接口，用户可以使用 FPC 排线将该接口连接到 CAM8000-A 模块。完成通用模拟摄像头的扩展。也可以在此接口定义上做转接板扩展自己需要的数字摄像头。此接口的详细定义见下表。

Pin	Name	Function explanation
1	GND	GND
2	D0	Digital image data bit 0
3	D1	Digital image data bit 1
4	D2	Digital image data bit 2
5	D3	Digital image data bit 3
6	D4	Digital image data bit 4
7	D5	Digital image data bit 5
8	D6	Digital image data bit 6
9	D7	Digital image data bit 7
10	D8	Digital image data bit 8

11	D9	Digital image data bit 9
12	D10	Digital image data bit 10
13	D11	Digital image data bit 11
14	GND	GND
15	PCLK	Pixel clock
16	GND	GND
17	HS	Horizontal synchronization
18	VDD50	5V
19	VS	Vertical synchronization
20	VDD33	3.3V
21	XCLKA	Clock output a
22	XCLKB	Clock output b
23	GND	GND
24	FLD	Field identification
25	WEN	Write Enable
26	STROBE	Flash strobe control signal
27	SDA	IIC2 master serial clock
28	SCL	IIC2 serial bidirectional data
29	GND	GND
30	VDD18	1.8V

180-pin 连接器

Mini8100核心板包含两个90Pin的插针连接器(间距:1.27mm).

连接器CON1的接口定义如下所示:

Pin	Name	Type	Function explanation
1	G_NWE	O	GPMC Write Enable
2	G_NOE	O	GPMC Read Enable
3	G_NCS7	O	GPMC Chip Select bit 7
	GPT8	IO	PWM or event for GP timer 8
	G_DIR	O	GPMC IO direction control for use with external transceivers
4	G_NCS4	O	GPMC Chip Select bit 7
	GPT9	IO	PWM or event for GP timer 9
	DMAREQ1	I	External DMA request 1
5	G_NCS6	O	GPMC Chip Select bit 7
	GPT11	IO	PWM or event for GP timer 11
	DMAREQ3	I	External DMA request 3
6	G_NCS3	O	GPMC Chip Select bit 7
	DMAREQ0	I	External DMA request 0
7	GND	GND	GND
8	G_WAIT0	I	External indication of wait
9	G_NBE0 / G_CLE	O	Lower Byte Enable. Also used for Command Latch Enable
10	G_NATV_ALE	O	Address Valid or Address Latch Enable
11	G_NBE1	O	Upper Byte Enable

12	HDQ_SIO	IOD	Bidirectional HDQ 1-Wire control and data
13	MMC1_D0	IO	MMC/SD Card Data bit 0
14	MMC1_D1	IO	MMC/SD Card Data bit 1
15	MMC1_D2	IO	MMC/SD Card Data bit 2
16	MMC1_D6/IO128	IO	MMC/SD Card Data bit 6
17	MMC1_D5/IO127	IO	MMC/SD Card Data bit 5
18	MMC1_D4/IO126	IO	MMC/SD Card Data bit 4
19	MMC1_D7/IO129	IO	MMC/SD Card Data bit 7
20	MMC1_D3	IO	MMC/SD Card Data bit 3
21	GND	GND	GND
22	MMC1_CLK	O	MMC/SD Output Clock
23	MMC1_CMD	IO	MMC/SD command signal
24	VMMC1	P	Power supply for SD/MMC1 (3.0 / 1.8V)
25	UART3_RX_IRRX	I	UART3 Receive data, IR and Remote RX
26	UART3_CTS_RCTX	IO	UART3 Clear To Send, Remote TX
27	UART3_TX_IRTX	O	UART3 Transmit data, IR TX
28	UART3_RTS_SD	O	UART3 Request To Send, IR enable
29	DSS_ACBIAS	O	AC bias control (STN) or pixel data enable (TFT) output
30	DSS_VSYNC	O	LCD Vertical Synchronization
31	GND	GND	GND
32	DSS_HSYNC	O	LCD Horizontal Synchronization
33	DSS_CLK	O	LCD Pixel Clock
34	DSS_D6	IO	LCD Pixel Data bit 6
35	DSS_D8	IO	LCD Pixel Data bit 8
36	DSS_D7	IO	LCD Pixel Data bit 7
37	DSS_D9	IO	LCD Pixel Data bit 9
38	DSS_D20	IO	LCD Pixel Data bit 20
39	DSS_D17	IO	LCD Pixel Data bit 17
40	DSS_D16	IO	LCD Pixel Data bit 16
41	DSS_D18	IO	LCD Pixel Data bit 18
42	DSS_D10	IO	LCD Pixel Data bit 10
43	DSS_D5	IO	LCD Pixel Data bit 5
44	DSS_D4	IO	LCD Pixel Data bit 4
45	GND	GND	GND
46	DSS_D2	IO	LCD Pixel Data bit 2
47	DSS_D3	IO	LCD Pixel Data bit 3
48	DSS_D0	IO	LCD Pixel Data bit 0
49	DSS_D15	IO	LCD Pixel Data bit 15
50	DSS_D11	IO	LCD Pixel Data bit 11
51	DSS_D23	IO	LCD Pixel Data bit 23
52	DSS_D22	IO	LCD Pixel Data bit 22
53	DSS_D14	IO	LCD Pixel Data bit 14

54	DSS_D19	IO	LCD Pixel Data bit 19
55	DSS_D13	IO	LCD Pixel Data bit 13
56	DSS_D21	IO	LCD Pixel Data bit 21
57	DSS_D1	IO	LCD Pixel Data bit 1
58	DSS_D12	IO	LCD Pixel Data bit 12
59	GND	GND	GND
60	MCBSP1_FSR/IO157	IO	Receive frame synchronization
61	MCBSP1_CLKR/IO156	IO	Receive Clock
62	MCBSP1_FSX/IO161	IO	Transmit frame synchronization
63	MCBSP1_CLKS/IO160	I	External clock input
64	MCBSP1_CLKX/IO162	IO	Transmit clock
65	MCBSP1_DR/IO159	I	Received serial data
66	MCBSP1_DX/IO158	IO	Transmitted serial data
67	GND	GND	GND
68	TV_OUTC	O	TV analog output S-VIDEO: TV_OUT2
69	TV_OUTY	O	TV analog output Composite: TV_OUT1
70	VDD33	P	Power supply for camera (3.3V 500mA)
71	IIC3_SCL	IODU	I2C Master Serial clock. Output is open drain
72	IIC3_SDA	IODU	I2C Serial Bidirectional Data. Output is open drain
73	IO25	IO	General-purpose IO 183
74	IO27	IO	General-purpose IO 183
75	BOOTJUMP	I	Boot configuration mode bit 5.
76	GND	GND	GND
77	VBUS	P	VBUS power rail (5V 10mA)
78	USB_DN	IO	USB Data N
79	USB_ID	I	USB ID
80	USB_DP	IO	USB Data P
81	PWM0	O	Pulse width driver 0
82	KR0	I	Keypad row 0
83	KR1	I	Keypad row 1
84	KR2	I	Keypad row 2
85	KR3	I	Keypad row 3
86	KR4	I	Keypad row 4
87	VDD18	P	Power supply from TPS65930 (VIO 1.8V)
88	GND	GND	GND
89	VDD18	P	Power supply from TPS65930 (VIO 1.8V)
90	BKBAT	P	Backup battery

连接器CON2的接口定义如下所示:

Pin	Name	Type	Function explanation
1	GND	GND	GND
2	G_D14	IO	GPMC data bit 14

3	G_D13	IO	GPMC data bit 13
4	G_D10	IO	GPMC data bit 10
5	G_D8	IO	GPMC data bit 8
6	G_D9	IO	GPMC data bit 9
7	G_D5	IO	GPMC data bit 5
8	G_D7	IO	GPMC data bit 7
9	G_D3	IO	GPMC data bit 3
10	G_D6	IO	GPMC data bit 6
11	G_D12	IO	GPMC data bit 12
12	G_D2	IO	GPMC data bit 2
13	G_D11	IO	GPMC data bit 11
14	G_D1	IO	GPMC data bit 1
15	G_D4	IO	GPMC data bit 4
16	G_D0	IO	GPMC data bit 0
17	G_A2	O	GPMC address bit 2
18	G_A3	O	GPMC address bit 3
19	G_A1	O	GPMC address bit 1
20	G_A6	O	GPMC address bit 6
21	G_A4	O	GPMC address bit 4
22	G_A7	O	GPMC address bit 7
23	G_A5	O	GPMC address bit 5
24	G_A8	O	GPMC address bit 8
25	G_A9	O	GPMC address bit 9
26	G_D15	IO	GPMC data bit 15
27	G_A10	O	GPMC address bit 10
28	GND	GND	GND
29	SPI2_CS1	O	SPI Enable 1
	GPT8	IO	PWM or event for GP timer 8
30	SPI2_CS10	IO	SPI Enable 0
	GPT11	IO	PWM or event for GP timer 11
31	SPI2_SIMO	IO	Slave data in, master data out
	GPT9	IO	PWM or event for GP timer 9
32	SPI2_CLK	IO	SPI Clock
33	SPI2_SOMI	IO	Slave data out, master data in
	GPT10	IO	PWM or event for GP timer 10
34	SPI1_CS3	O	SPI Enable 3
35	SPI1_CS0	IO	SPI Enable 0
36	SPI1_SIMO	IO	Slave data in, master data out
37	SPI1_SOMI	IO	Slave data out, master data in
38	SPI1_CLK	IO	SPI Clock
39	GND	GND	GND
40	GPIO0	IO	GPIO0 /card detection 1
41	MMC2_D2	IO	MMC/SD Card Data bit 2

	SPI3_CS1	O	SPI Enable 1
42	MMC2_D3	IO	MMC/SD Card Data bit 3
	SPI3_CS0	IO	SPI Enable 0
43	MMC2_D0	IO	MMC/SD Card Data bit 0
	SPI3_SOMI	IO	Slave data out, master data in
44	MMC2_D1	IO	MMC/SD Card Data bit 1
45	MMC2_CMD	IO	MMC/SD command signal
	SPI3_SIMO	IO	Slave data in, master data out
46	MMC2_CLK	O	MMC/SD Output Clock
	SPI3_CLK	IO	SPI Clock
47	BSP3_DR	I	Received serial data
	UART2_RTS	O	UART2 Request To Send
48	BSP3_CLK	IO	Combined serial clock
	UART2_TX	O	UART2 Transmit data
49	BSP3_FSX	IO	Combined frame synchronization
	UART2_RX	I	UART2 Receive data
50	BSP3_DX	IO	Transmitted serial data
	UART2_CTS	I	UART2 Clear To Send
51	GND	GND	GND
52	UART1_CTS	I	UART1 Clear To Send
53	UART1_TX	O	UART1 Transmit data
54	UART1_RX	I	UART1 Receive data
55	UART1_RTS	O	UART1 Request To Send
56	USB1HS_STP	O	Dedicated for external transceiver Stop signal
57	USB1HS_D3	IO	Dedicated for external transceiver Bidirectional data bus
58	USB1HS_D5	IO	Dedicated for external transceiver Bidirectional data bus
59	USB1HS_6	IO	Dedicated for external transceiver Bidirectional data bus
60	USB1HS_D7	IO	Dedicated for external transceiver Bidirectional data bus
61	USB1HS_D1	IO	Dedicated for external transceiver Bidirectional data bus
62	USB1HS_D2	IO	Dedicated for external transceiver Bidirectional data bus
63	USB1HS_D4	IO	Dedicated for external transceiver Bidirectional data bus
64	USB1HS_D0	IO	Dedicated for external transceiver Bidirectional data bus
65	USB1HS_NXT	I	Dedicated for external transceiver Next signal from PHY
66	USB1HS_CLK	O	Dedicated for external transceiver 60-MHz clock
67	GND	GND	GND
68	USB1HS_DIR	I	Dedicated for external transceiver data form PHY
69	SYS_CLKOUT1	O	Configurable output clock1
70	LEDA	OD	LED leg A
71	LEDB	OD	LED leg B

72	ADCIN0	AI	ADC input0 (Battery type)
73	NRESPWRON	I	Power On Reset
74	NRESWARM	IODU	Warm Boot Reset (open drain output)
75	SYSEN	ODU	System enable output
76	GND	GND	GND
77	REGEN	ODU	Enable signal for external LDO
78	ADCIN1	AI	ADC input1 (General-purpose ADC input)
79	KC0	OD	Keypad column 0
80	KC1	OD	Keypad column 0
81	KC2	OD	Keypad column 0
82	KC3	OD	Keypad column 0
83	AUDIO_IN	AI	Analog microphone bias 1
84	AUDIO_OR	A0	Predriver output right P for external class-D amplifier
85	AUXR	AI	Auxiliary audio input right
86	AUDIO_OL	A0	Predriver output left P for external class-D amplifier
87	GND	GND	GND
88	VBAT	P	Power supply (3V - 4.2V 1.5A)
89	ON/OFF	I	Input; detect a control command to start or stop the system
90	VBAT	P	Power supply (3V - 4.2V 1.5A)

注: 上表中 Type 的定义如下:

I: Input

O: Output

A: Analog signal

P: Power

D: Open Drain

U: Pull-up resistor

GND: Power ground

订购信息

订单编号.	T400142
名称	Mini8100 核心板
光盘资料	<ul style="list-style-type: none"> ● WinCE、Linux 镜像文件 ● 用户手册 ● PDF 原理图

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